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REMARKS

Claims 1, 6-8, 10, 13, 22, 26, 29, and 31are amended, no claims are canceled, and claims 32-39 are added; as a result, claims 1, 2, 4-8, 10-23, 25-27 and 29-39 are now pending in this application.

Amendments to Claims

The amendments to claims 1, 6-8, 1, 13, 22, 26, 29, and 31 were made to facilitate prosecution of the claims in light of rejections previously made in a Final Office Action, dated June 26, 2002, for the parent application. Each of the previous rejections is addressed, below.

Rejections Under 35 U.S.C.§102

Rejection based on Ito (U.S. Patent No. 5,648,910):

Claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31 were rejected under 35 U.S.C.§102(b) as being anticipated by Ito (U.S. Patent No. 5,648,910). Applicant has amended claims 1, 7, 13, 22, 26, 29, and 31 to more clearly distinguish Applicant's invention from that which is disclosed by Ito. Based on these amendments and the remarks, below, Applicant believes that claims 1, 7, 13, 22, 26, 29, and 31 (and claims 2, 4, 6, 8, 10-12, 14-17, 23, 25, 27, and 30, which depend therefrom) are in a condition for allowance.

Ito discloses a method of optimizing a power supply network, wherein portions of the method are performed by a CAD system. The CAD system receives interconnecting data and test vector data, and estimates current consumption for each function block. (See Fig. 2, block S2; and col. 4, lines 60-62). The CAD system produces a current consumption map (See Fig. 4), which roughly indicates the magnitudes of the current consumption within various areas of the circuit using contour lines. (See Fig. 2, block S3; Fig. 4; and col. 5, lines 8-21). The CAD system then determines appropriate routes of power supply lines of a power supply network. (See Fig. 2, block S5; and col. 5, lines 43-45).

The power supply network includes power supply sub-lines (Fig. 7, elements 14 and 18 (subscripts removed)), which transfer positive voltage and ground to various function blocks (Fig. 7, blocks 20-24). The power supply sub-lines extend over the function blocks. (Fig. 7; and

col. 6, lines 47-61). The CAD system calculates the amount of current passing through each of the power supply sub-lines, and changes the width of the power supply sub-line if the amount of current is too large to prevent the power supply sub-line from electromigration. (Fig. 2, blocks S8, S9; and col. 6, line 62 through col. 7, line 1). If a power supply sub-line is too wide to form over the semiconductor chip, the designer requests the CAD system to rearrange the floor plan. (See Fig. 2, block S10; and col. 7, lines 10-12). The procedure is then repeated, until all the power supply sub-lines become feasible. (col. 7, lines 14-16).

Applicant's claims 1, 7, 13, 22, 26, 29, and 31 (and claims 2, 4, 6, 8, 10-12, 14-17, 23, 25, 27, and 30, which depend therefrom) include at least the following limitations, which distinguish these claims over Ito:

Limitations of Applicant's Claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31	Ito (U.S. Patent No. 5,648,910)
". . . <u>if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce a revised circuit layout</u>. . ." (claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31 – claim language may vary slightly)	In the method of Ito, the CAD system compensates for electromigration by changing the width of power supply sub-lines. (Fig. 2, blocks S8, S9; and col. 6, line 62 through col. 7, line 1). If a power supply sub-line is too wide to form over the semiconductor chip, *the designer* requests the CAD system to rearrange the floor plan. (See Fig. 2, block S10; and col. 7, lines 10-12). Therefore, the only automatic process that occurs as a result of the CAD system detecting an electromigration problem is the alteration of a wire width. Portions of the circuit layout are not automatically rearranged using the method of Ito. Rearrangement and re-evaluation of the circuit layout is initiated only by intervention of a human (the designer).

Rejection based on Hathaway et al. (U.S. Patent No. 5,737,580):

Claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31 were rejected under 35 U.S.C.§102(b) as being anticipated by Hathaway et al. (U.S. Patent No. 5,737,580). Applicant has amended claims 1, 7, 13, 22, 26, 29, and 31 to more clearly distinguish Applicant's invention from that which is disclosed by Hathaway et al.. Based on these amendments and the remarks, below, Applicant believes that claims 1, 7, 13, 22, 26, 29, and 31 (and claims 2, 4, 6, 8, 10-12, 14-17, 23, 25, 27, and 30, which depend therefrom) are in a condition for allowance.

Hathaway et al. disclose a method for wiring IC chips such that electromigration (EM) criteria are met. (See Abstract). An automatic placement tool is executed for initial circuit placement, and estimated net configurations are developed. (Fig. 4, block 230; and col. 4, lines 38-40). An EM checker performs EM checking on the estimates. (Fig. 4, block 292; and col. 4, lines 40-41). Using a capacitance target file produced by the EM checker, the placement tool is re-executed, along with the EM checker. To compensate for identified EM errors, wire widths are increased in the model until the EM errors are eliminated. (col. 4, lines 43-55).

Applicant's claims 1, 7, 13, 22, 26, 29, and 31 (and claims 2, 4, 6, 8, 10-12, 14-17, 23, 25, 27, and 30, which depend therefrom) include at least the following limitations, which distinguish these claims over Hathaway et al.:

Limitations of Applicant's Claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31	Hathaway et al. (U.S. Patent No. 5,737,580)
". . . if the analysis indicates that the circuit layout does not satisfy a rule of the at least one layout rule, automatically rearranging portions of the circuit layout, to produce a revised circuit layout. . ." (claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31 – claim language may vary slightly)	In the method of Hathaway et al., the CAD system compensates for electromigration by increasing wire widths in the model until the EM errors are eliminated. (col. 4, lines 43-55). Therefore, the only automatic process that occurs as a result of the CAD system detecting an electromigration problem is the alteration of a wire width. Portions of the circuit layout are not automatically rearranged using the method of Hathaway et al..

Based on the amendments and the above remarks, Applicant believes that claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31 are distinguishable from Ito and from Hathaway et al., and that these claims are allowable. Accordingly, Applicant respectfully requests that the Examiner allow claims 1-2, 4, 6-8, 10-17, 22-23, 25-27, and 29-31.

Rejections Under 35 U.S.C.§103

Claim 5 was rejected under 35 U.S.C.§103(a) as being unpatentable over Ito (U.S. Patent No. 5,648,910). In addition, claim 5 was rejected under 35 U.S.C.§103(a) as being unpatentable over Hathaway et al. (U.S. Patent No. 5,737,580). Applicant has addressed each of these references in conjunction with the remarks regarding the rejection of the claims under 35 U.S.C. § 102(b). In addition, Applicant has amended claim 1, from which claim 5 depends, to more clearly differentiate claim 1 from Ito and Hathaway et al.. Accordingly, Applicant believes that the rejections of claim 5 under 35 U.S.C.§103(a) are now moot, and that claim 5 is in a condition for allowance. Applicant respectfully requests that the Examiner allow claim 5.

Claims 18-21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Hathaway et al. (U.S. Patent No. 5,737,580) in view of Gupta et al., "Optimal 2-D Cell Layout with Integrated Transistor Folding", 1998 IEEE/ACM International Conference on Computer-Aided Design, 8 November 1998, pp. 128-135). Applicant has amended claim 13, from which claims 18-21 depend, in order to more clearly distinguish Applicant's invention from that which is disclosed by Hathaway et al.. Accordingly, the amendment to claim 13 has the effect that claims 18-21 are now more clearly distinguished from that which is disclosed by Hathaway et al.. Further, claims 18-21 are distinguishable from the combination of Hathaway et al. and Gupta et al.. Based on the amendment to claim 13 and the remarks, below, Applicant believes that claims 18-21 are in a condition for allowance.

Gupta et al. disclose a method for folding transistors within a set of transistors, whose sizes exceed a predetermined maximum. (See col. 3, lines 10-14). Gupta et al. do not discuss electromigration or self heat issues.

Claims 18-21 are dependent on claim 13 (claim 14 is intervening). As discussed above, Applicant's believe that claim 13 is distinguishable over that which is disclosed in Hathaway et

al.. Further, neither Hathaway et al. nor Gupta et al. indicate that there is a motivation to combine these references.

For these reasons, Applicant believes that claims 18-21 are distinguishable over the combination of Hathaway et al. and Gupta et al. Accordingly, Applicant respectfully requests that the Examiner allow claims 18-21.

Support for Claim Amendments

The amendments to the claims are supported in the Specification and Figures as listed below. No new matter is introduced as a result of these amendments.

Claim 1: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 6: The amendment corrects antecedent basis, thus no limitations have been added or removed.

Claim 7: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 8: The amendment corrects antecedent basis, thus no limitations have been added or removed.

Claim 12: The amendment corrects antecedent basis, thus no limitations have been added or removed.

Claim 13: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 22: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 26: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 29: Figure 13, and page 17, line 28 through page 18, line 23.

Claim 31: Figure 13, and page 17, line 28 through page 18, line 23.

Support for New Claims

New claims 32-39 are supported in the Specification and Figures as listed below. No new matter is introduced as a result of these claims:

Claim 32: Figures 1A, 1B, 2A, and 2B, and page 6, lines 22-26.

Claim 33: Figure 5, and page 9, line 10 through 26.

Claim 34: Figures 5 and 6, and page 9, line 10 through page 10, line 4.

Claim 35: Figure 13, block 1306, and page 18, lines 7-9.

Claim 36: Figure 6, and page 9, line 21 through page 10, line 4.

Claim 37: Figure 8, and page 14, lines 3-14.

Claim 38: Figure 15, and page 21, line 21 through page 22, line 15.

Claim 39: Figure 5, block 502, Figure 6, block 602, and page 9, lines 27-29.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Sherry Schumm at (480) 657-3766, or the below signed attorney to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully Submitted,

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CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelop addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 24 day of July 2003

Name Emily Bates Signature Emily Bates